ICD Integrated Circuit Design Lab

GF METRC GSME FAST Microelectronics Training & Research Center

THE BRIDGE OF HOPE

IC DESIGN SUMMER SCHOOL - 2025
IN FAST NATIONAL UNIVERSITY

Six-Week Internship in Integrated Circuit (IC) Design at ICD Lab of Fast National University Islamabad

OBJECTIVE

- Strengthen IC Design Ecosystem in Pakistan
- Prepare Students for Final Year Projects.
- Exposure to National & International Industrial Experts.
- Bridging the Connection Between Local Industry & Students.
- Training of Students & Young Faculty in Area of IC Design.

Timing & Schedule

Lectures - 09:00 am to 12:00 pm
Hands on Lab Tutorial - 01:30 pm to 4:30 pm

Program Duration

Six-Week Paid Internship
16 June 2025- 25 July 2025

SALIENT FEATURES

HANDS-ON IC DESIGN

Tutorials and Labs on industry standard **Cadance Tools Suite** & Advanced PDKs

EXPERIENCED TRAINERS

All Instructors Have Hands-on Experience in IC Design

INTERNATIONAL EXPOSURE

Guest Speakers from **NVIDIA, Samsung, Synopsys & GSME**

ICD Integrated Circuit Design Lab | 10X ENGINEERING | π Invent Dos IP Kapital | GS MICRO ELECTRONICS

National University Of Computer and Emerging Sciences

LAST DATE TO APPLY: 05 JUNE 2025

For Queries or further information contact:
Email: usama.mustafa@isb.nu.edu.pk
Contact No: 0306-8905225

APPLY ONLINE AT FOLLOWING GOOGLE FORM LINK/ SCAN QR

FAST ICD Lab Summer Internship Application

VISIT OUR WEBSITE:
FAST ICD LAB

Guest Speakers
Insights from Chip Design Industry

Dr. Imtinan Elahi

Principal Mixed Signal Design Engineer, NVIDIA.

Modeling of end-end high-speed wired and wireless communication systems for design and verification; link budget analysis; hardware implementation of DSP blocks.

Dr. Noman Hai

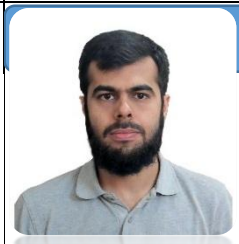
Sr. Manager Synopsys, Canada

His doctoral research centered on CMOS analog-to-digital converters, and he has deep expertise in high-speed analog circuit design. Currently a Senior Analog Design Manager at Synopsys Canada, he leads 224Gb/s SerDes development and holds three U.S patents.

Dr. Atheer Barghouthi

Director of Design Engineering at GSME Inc. Oman.

He brings decades of hands-on experience in chip and block-level IC design and layout. His tapeouts span a wide range of analog, RF, and mixed-signal.



Dr. Zain-ul-Abideen

Asst. Professor at University of Idaho, USA.

He focus on hardware security, secure IC design, EDA, hardware Trojans, reverse engineering, PUFs, TRNGs. He has contributed to NSF and EU Horizon-funded projects.

Dr. Bilal Zafar

CEO 10x Engineering, Lahore

He has proven ability to create and implement solutions in an emerging SoC industry in Pakistan by building, growing, and leading high-performance engineering teams.

Dr. Nasir Mohyuddin

Deputy Director General (DDG) and Head of National IC Design Center @ NECOP, Pakistan

He oversees RF, digital, analog, and mixed-signal IC design using Cadence and Synopsys tools, along with IC failure analysis support, & also developed Pakistan's first industrial-grade RISC-V based indigenous embedded processor & its software ecosystem

Dr. Rashid Iqbal

Senior Principal Application Engineer at Cadence, USA.

He has over 24 years of experience specializing in physical design and advanced SoC implementation. He also runs a YouTube channel that simplifies digital logic, CMOS, and IC implementation concepts for students and engineers.

Dr. Rehan Ahmed

Director of Hardware Engineering DreamBig Semiconductor, Islamabad.

He specializes in FPGA development, custom IP, and digital IC design. He led Pakistan's first silicon proven RISC-V microprocessor project and now directs global hardware teams at DreamBig Semiconductor.

Dr. Muhammad Afzal

Chief Technical Engineer at Arcean Semiconductor, Islamabad

He has over 30 years of experience in specializing in FPGA development, Digital ICs front-end design, back-end, Custom Ip development, design Verification, Systems on chip, and product development.

Dr. Yasir Qadri

Director Computer Architecture & Engineering, NECOP, Pakistan

He earned PhD from the University of Essex, UK. He has received numerous funding's for his work in Microprocessor Design and possesses over two decades of hands-on experience in hardware security, Multicore Processor Design, and SoC development.

Instructors

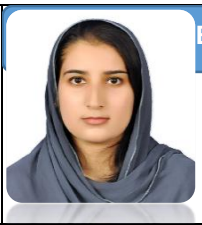
Dr. Rashid Ramzan

Professor of EE, Director ICD Lab, & CEO Pi-Invent.

IC Design lab was established in 2018, Our lab has produced 70+ highly skilled engineers with degree in MS IC Design. Dr. Ramzan, has over 10 years of industrial and over 15 years of academic experience with more than 100 journal & conference publication and 12 granted US Patents and two chancellor innovation awards.

Dr. Hassan Saif

Power Management and Harvesting IC Design

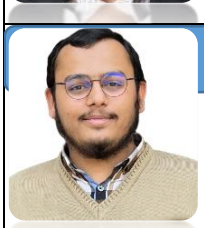


Engr. Aqsa Ehsan

Lecturer
MS RF Electronics

Engr. Riffat Tahira

Lab Engineer
MS. IC Design



Engr. Hamza

Design Engineer
MS IC Design

Engr. Adeel

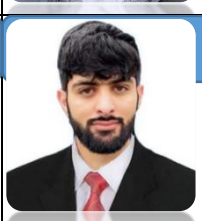
Design Engineer
MS IC Design

Engr. Sagheer

Design Engineer
MS IC Design

Engr. Nouman

Design Engineer
MS IC Design



Engr. Atif Khan

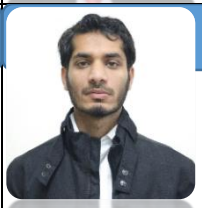
Design Engineer
MS IC Design

Engr. Mubeen

Design Engineer
MS IC Design

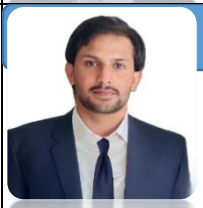
Engr. Ahmed

Design Engineer
MS IC Design



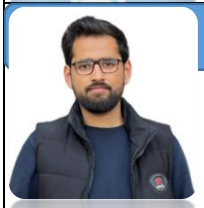
Engr. M Yousaf

Design Engineer
MS IC Design



Engr. Sana Ullah

Design Engineer
MS IC Design



Engr. Rohail

Design Engineer
MS IC Design

Engr. Saleh

Design Engineer
MS IC Design

Engr. Hafiz Azeem

Design Engineer
MS IC Design

Engr. Abira Malik

Design Engineer
MS IC Design

Engr. M Mujahid

Design Engineer
MS IC Design

Engr. Asad Tariq

Design Engineer
MS IC Design

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Timing & Schedule

The IC Design Internship program will run for ***06 weeks, 05 days a week***, following the schedule and timings of lectures and lab work outlined below:

Gusts Lectures/ Theory Classes	Labs & Lab Assignments
○ **1st** - 09:00 am – 10:15 am ○ **2nd** - 10:45 am – 12:00 pm	○ 1:30 pm – 4:30 pm

Program Outline

Weeks	Guest Lectures/ Theory	Labs	Instructors
1st	Guest Talk: Insights from Chip Design Industry ***Regular Classes: Introduction to IC Design*** ○ Introduction to Internship Program ○ Why IC Design? ○ Revision of Semiconductor Physics ○ PN Junction ○ Transistor, a marvellous device ever invented! ○ CMOS Fabrication Process	○ Lab-Tutorials & Lab Assignments, and Quizzes	1. Rashad Ramzan 2. Hassan Saif 3. Adeel Ahmed 4. Ahmed Aljellani 5. Hamza Sadiq 6. Sagheer Abbas 7. Mubeen Yousaf 8. Rohail Ahmed 9. Saleh Sherazi 10. Nouman Ahmed 11. Hafiz Azeem 12. M. Yousaf 13. M. Atif 14. Sana-Ullah 15. Mujahid Iqbal 16. Riffat Taira 17. Abira Malik 18. Asad Tariq
2nd	Guest Talk: Insights from Chip Design Industry ***Regular Classes: Basics of CMOS Amplifier.*** ○ Current Sources Amplification Process ○ Common Source Amplifier, Source Degeneration ○ Common Gate Amplifier ○ Common Drain Amplifier ○ Current Source Amplifier	○ Lab-Tutorials & Lab Assignments, and Quizzes ○ Soft Skills Demo	
3rd	Guest Talk: Insights from Chip Design Industry ***Regular Classes: Differential & Multistage Amplifier*** ○ Differential Pair with Passive Load ○ Differential Pair with Active Load ○ Multistage Amplifier Design ○ Frequency Response ○ Feedback Circuits	○ Lab-Tutorials & Lab Assignments, and Quizzes	
4th	Guest Talk: Insights from Chip Design Industry ***Regular Classes: CMOS Inverter & Inverter Chain*** ○ Inverter VTC ○ Inverter Static Behaviour ○ Inverter Transient Response ○ Inverter Noise Limits ○ Inverter Chain Design ○ Inverter Power Analysis	○ Lab-Tutorials & Lab Assignments, and Quizzes	
5th	Guest Talk: Insights from Chip Design Industry ***Regular Classes: Combinational Logic*** ○ Design Multi Input Logic Gates ○ Basic Logic Gate Design & Optimization ○ Complex Logic Function CMOS Implementation & Optimization ○ Combinational Logic Design & Optimization	○ Lab-Tutorials & Lab Assignments, and Quizzes ○ Soft Skills Demo	
6th	Guest Talk: Insights from Chip Design Industry ***Regular Classes: Interconnections & Sequential Elements*** ○ CMOS Latch Design ○ Interconnect Models in Inverter ○ Bistability CMOS ○ Interconnect Delay Models ○ Couplings & Crosstalk ○ Elmore Delay ○ CMOS Combinational Logic Delay Including Interconnect Delay	○ Lab-Tutorials & Lab Assignments, and Quizzes ○ Certificate Distribution	

FAST-NU ICD SUMMER SCHOOL 2025

Rules & Regulations

Eligibility Criteria

Students must meet the following requirements to be considered for the IC Design Summer Internship 2025:

- **Eligibility: Completed Coursework** in the following subjects:
  - Signals & Systems
  - Electronics-I (Semiconductor Physics & PN Junction)
  - Electronics-II (CMOS transistor, Frequency Response, & Feedback Concepts)
- **Target Audience**:
  - Electrical Engineering & Relevant Discipline 6th Semester Students Planning to take IC Design Final Year Project.
  - Electrical Engineering Faculty Members & Lab Engineers especially related to Electronics & IC Design Graduate/Undergraduate Programs.
- **Application Process & Requirements**:
  - Apply at Google Form application Link (https://forms.gle/r2fx4BBQvURap6Wc7) Candidates meeting the above criteria will be shortlisted for an interview.
  - Your genuine commitment is paramount. To ensure a true reflection of your passion, a handwritten motivational letter is mandatory. This letter must be entirely your own work, with absolutely no assistance from AI generation. Any submission identified as AI-generated will result in disqualification.
- **Scholarship & Stipend**
  - ***Deserving Students*** will receive a stipend of Rs. 20,000/- upon successful completion of the internship.
- **Your Commitment, Our Resources & Efforts:**
  - This program offers valuable access to Cadence Tools Suite, Computing Resources, and expert-led training, completely free of charge.
  - To ensure these resources are utilized effectively, we seek only participants with a genuine passion for IC design and a strong commitment to completing the program.
  - Therefore, your commitment is needed to ensure that you will complete this internship.
    - Selected students are required to submit a refundable security deposit of Rs. 18,000/- **or** a Surety Letter from the Head of Department of respective university/ tentative FYP Supervisor mentioning he/she would not leave internship without completion.
    - The security deposit (if submitted) will be returned during the last week of internship, Security fee will be non-refundable if a candidate does not complete internship.